Parallel Input, 12-Bit Rail-to-Rail Micropower DACs in SSOP

FEATURES

- **Guaranteed Monotonic**
- **Buffered True Rail-to-Rail Voltage Output**
- 12-Bit Resolution
- 3V Operation (LTC1450L) I_{CC}: 250µA Typ
- 5V Operation (LTC1450) I_{CC}: 400µA Typ
- Parallel 12-Bit or 8 + 4-Bit Double Buffered Digital Input
- Internal Reference
- Output Buffer Configurable to Gain of 1 or 2
- Configurable as a Multiplying DAC
- Internal Power-On Reset
- **Maximum DNL Error: 0.5LSB**

APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Arbitrary Function Generators
- Battery-Powered Data Conversion Products
- Feedback Control Loops and Gain Control

DESCRIPTION

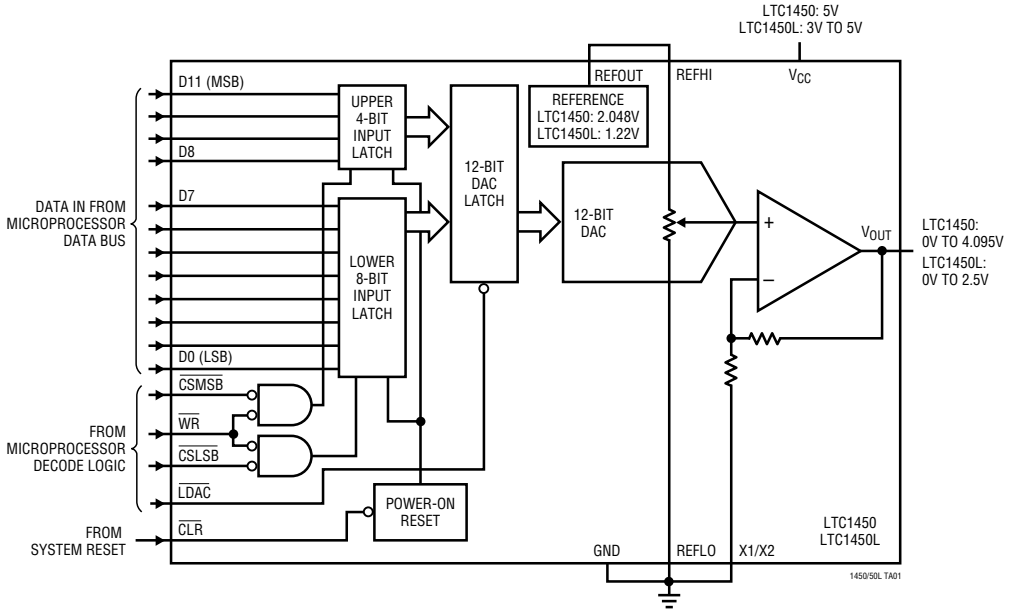
The LTC®1450/LTC1450L are complete single supply, rail-to-rail voltage output, 12-bit digital-to-analog converters (DACs) in a 24-pin SSOP or PDIP package. They include an output buffer amplifier, reference and a double buffered parallel digital interface.

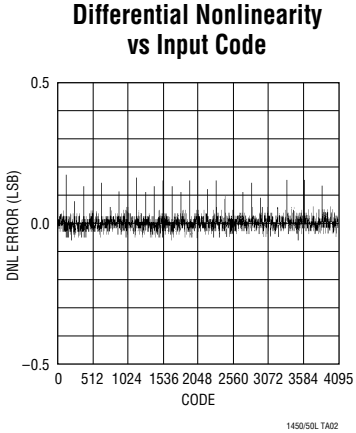
The LTC1450 operates from a 4.5V to 5.5V supply. The output can be pin strapped for 4.095V or 2.048V full-scale. It has a 2.048V internal reference.

The LTC1450L operates from a 2.7V to 5.5V supply. The output can be pin strapped for 2.5V or 1.22V full-scale. It has a 1.22V internal reference.

The LTC1450/LTC1450L offer true stand-alone performance. In addition, the reference output, high and low reference inputs and gain setting resistor are brought to pins for maximum flexibility.

TYPICAL APPLICATION

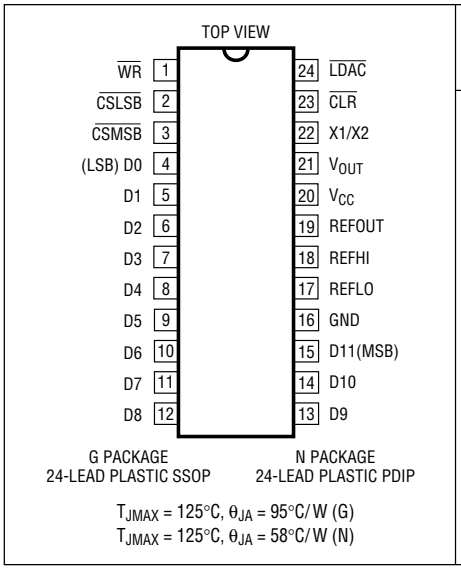




ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND ..... –0.5V to 7.5V
Logic Inputs to GND ..... –0.5V to 7.5V
V_{OUT} ..... –0.5V to V_{CC} + 0.5V
REFOUT, REFLO, REFHI, X1/X2 ..... –0.5V to V_{CC} + 0.5V
Maximum Junction Temperature ..... 125°C
Operating Temperature Range
Commercial ..... 0°C to 70°C
Industrial ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE
24-LEAD PLASTIC SSOP

N PACKAGE
24-LEAD PLASTIC PDIP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W (G)
T_{JMAX} = 125°C, θ_{JA} = 58°C/W (N)

ORDER PART NUMBER

LTC1450CG
LTC1450CN
LTC1450IG
LTC1450IN
LTC1450LCG
LTC1450LCN
LTC1450LIG
LTC1450LIN

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V (LTC1450), 2.7V to 5.5V (LTC1450L), V_{OUT} unloaded, REFOUT = REFHI, REFLO = GND = X1/X2, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	12			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 1)	●			±0.5	LSB
INL	Integral Nonlinearity	T_A = 25°C				±3.5	LSB
		(Note 1)	●			±4.0	LSB
V_{OS}	Offset Error	T_A = 25°C				±12	mV
			●			±18	mV
V_{OS} TC	Offset Error Temperature Coefficient				±15		µV/°C
V_{FS}	Full-Scale Voltage	Using Internal Reference, LTC1450, T_A = 25°C		4.065	4.095	4.125	V
		Using Internal Reference, LTC1450	●	4.045	4.095	4.145	V
		External 2.048V Reference, LTC1450	●	4.075	4.095	4.115	V
		Using Internal Reference, LTC1450L, T_A = 25°C		2.470	2.500	2.530	V
		Using Internal Reference, LTC1450L	●	2.460	2.500	2.540	V
		External 1.22V Reference, LTC1450L	●	2.480	2.500	2.520	V
V_{FS} TC	Full-Scale Voltage Temperature Coefficient	Using Internal Reference, LTC1450			±0.10		LSB/°C
		Using External Reference, LTC1450/LTC1450L			±0.02		LSB/°C
		Using Internal Reference, LTC1450L			±0.10		LSB/°C
Reference Output (REFOUT)							
	Reference Output Voltage	LTC1450L	●	1.195	1.220	1.245	V
		LTC1450	●	2.008	2.048	2.088	V
	Reference Output Temperature Coefficient				±0.08		LSB/°C
	Reference Line Regulation		●		0.7	±2	LSB/V
	Reference Load Regulation	$0 \le I_{OUT} \le 100\mu A$, LTC1450L	●		0.6	±3.0	LSB
		LTC1450	●		0.2	±1.5	LSB
	Short-Circuit Current	REFOUT Shorted to GND	●			80	mA

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V (LTC1450), 2.7V to 5.5V (LTC1450L), V_{OUT} unloaded, REFOUT = REFHI, REFLO = GND = X1/X2, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input (REFLO = GND)							
	REFHI Input Range	$V_{REFHI} \leq V_{CC} - 1.5V$	●			$V_{CC}/2$	V
	REFHI Input Resistance		●	8	18	30	kΩ
	REFHI Input Capacitance				15		pF
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance, LTC1450L	●	2.7		5.5	V
		LTC1450	●	4.5		5.5	V
I_{CC}	Supply Current	$4.5V \leq V_{CC} \leq 5.5V$ (Note 4) LTC1450	●	300	400	620	µA
		$2.7V \leq V_{CC} \leq 5.5V$ (Note 4) LTC1450L	●	150	250	500	µA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●			100	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●			120	mA
	Output Impedance to GND	Input Code = 0	●		40	120	Ω
AC Performance							
	Voltage Output Slew Rate	(Note 2)	●	0.5	1.0		V/µs
	Voltage Output Settling Time	(Notes 2, 3) to ±0.5LSB			14		µs
	Digital Feedthrough	LDAC = 1			5		(nV)(s)
	AC Feedthrough	REFHI = 1kHz, $2V_{P-P}$			–95		dB
SINAD	Signal-to-Noise + Distortion	REFHI = 1kHz, $2V_{P-P}$ (Code: All 1's)			85		dB
Digital Inputs							
V_{IH}	Digital Input High Voltage	V_{CC} = 3V, LTC1450L	●	2.2			V
		V_{CC} = 5V, LTC1450	●	2.4			V
V_{IL}	Digital Input Low Voltage	V_{CC} = 3V, LTC1450L	●			0.8	V
		V_{CC} = 5V, LTC1450	●			0.8	V
V_{LTH}	Logic Threshold Voltage	LTC1450L			$V_{CC}/2$		V
I_{LEAK}	Digital Input Leakage	V_{CC} = 5V, V_{IN} = GND to V_{CC}	●	–10		10	µA
C_{IN}	Digital Input Capacitance	Guaranteed by Design. Not Subject to Test	●			10	pF

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V (LTC1450), V_{CC} = 2.7V to 3.6V (LTC1450L), $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Characteristics (Note 5)							
t_{CS}	$\overline{CS}$ (MSB or LSB) Pulse Width		●	40			ns
t_{WR}	$\overline{WR}$ Pulse Width		●	40			ns
t_{CWS}	$\overline{CS}$ to $\overline{WR}$ Setup		●	0			ns
t_{CWH}	$\overline{CS}$ to $\overline{WR}$ Hold		●	0			ns
t_{DWS}	Data Valid to $\overline{WR}$ Setup	V_{CC} = 4.5V to 5.5V (LTC1450) V_{CC} = 2.7V to 3.6V (LTC1450L) V_{CC} = 5V (LTC1450L)	● ●	40 40	15 15 10		ns ns ns
t_{DWH}	Data Valid to $\overline{WR}$ Hold	V_{CC} = 4.5V to 5.5V (LTC1450) V_{CC} = 2.7V to 3.6V (LTC1450L) V_{CC} = 5V (LTC1450L)	● ●	0 0	–10 –10 –5		ns ns ns
t_{LDAC}	$\overline{LDAC}$ Pulse Width		●	40			ns
t_{CLR}	$\overline{CLR}$ Pulse Width		●	40			ns

The ● denotes specifications which apply over the full operating temperature range.

Note 1: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 4095 (full-scale).

Note 2: Load is 5kΩ in parallel with 100pF.

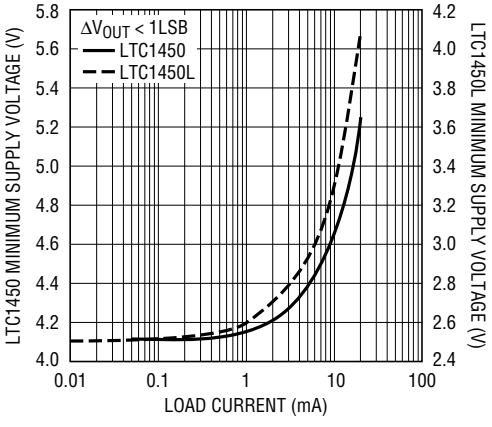
Note 3: DAC switched all 1's and the code corresponding to $V_{OS(MAX)}$ for the part.

Note 4: Digital inputs at 0V or V_{CC}.

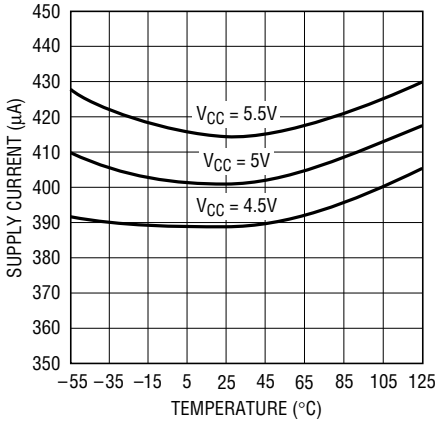
Note 5: Digital inputs swing 10% to 90% of V_{CC}, $t_r = t_f$ = 5ns and timing measurements are from $V_{CC}/2$.

TYPICAL PERFORMANCE CHARACTERISTICS

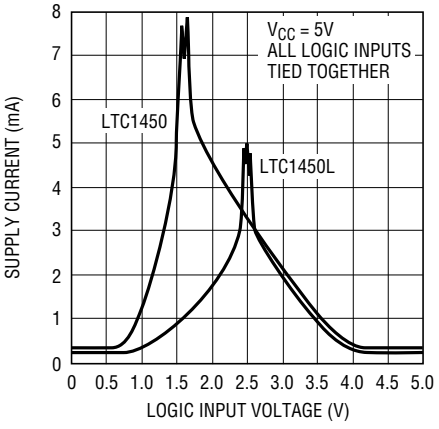
Minimum Supply Voltage vs Load Current



LTC1450 Supply Current vs Temperature

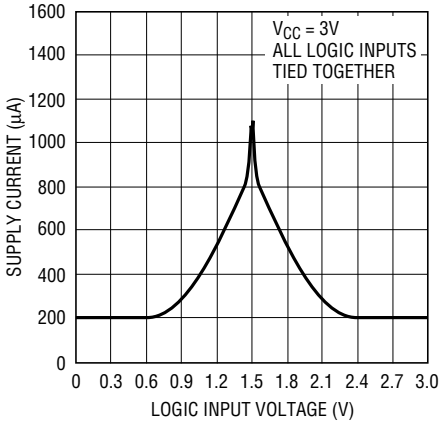


Supply Current vs Logic Input Voltage



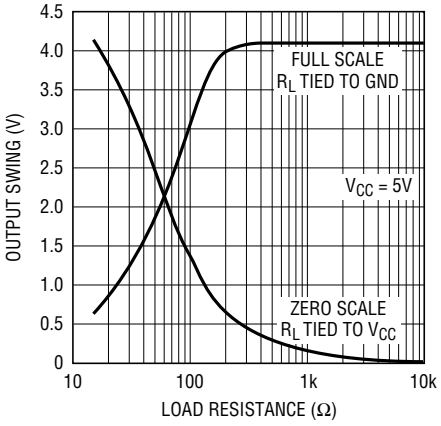
TYPICAL PERFORMANCE CHARACTERISTICS

LTC1450L Supply Current vs Logic Input Voltage



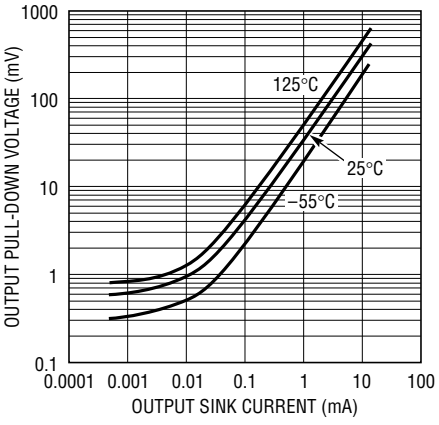
1450/50L G04

LTC1450 Output Swing vs Load Resistance



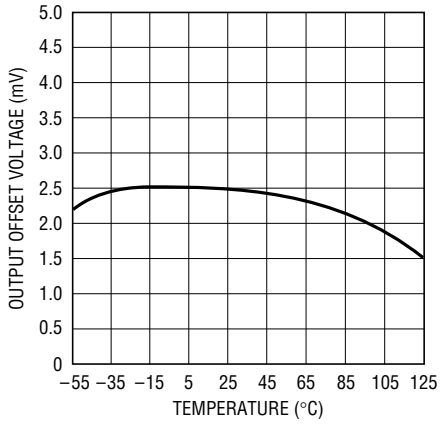
1450/50L G05

LTC1450 Pull-Down Voltage vs Output Sink Current Capability



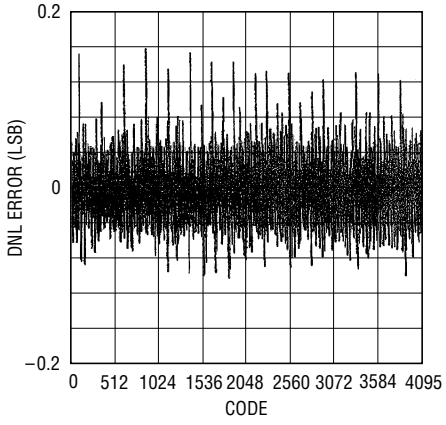
1450/50L G06

LTC1450 Output Offset Voltage vs Temperature



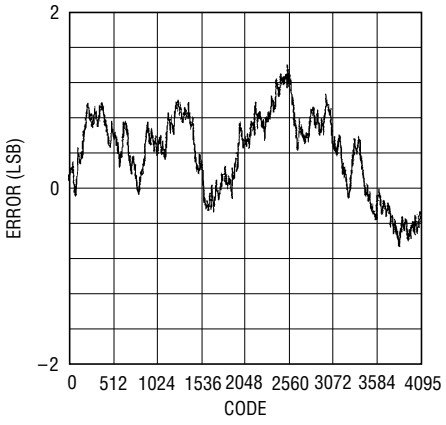
1450/50L G07

LTC1450 Differential Nonlinearity (DNL)



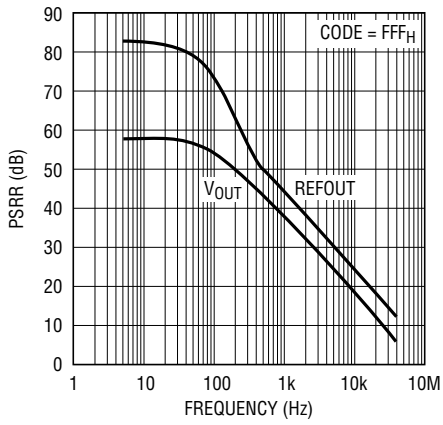
1450/50L G08

LTC1450 Integral Nonlinearity (INL)



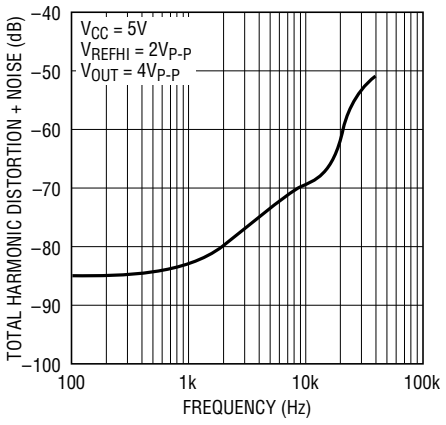
1450/50L G09

Power Supply Rejection vs Frequency



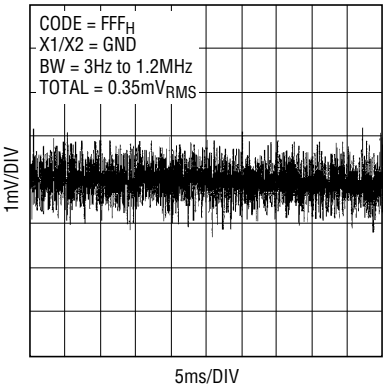
1450/50L G10

LTC1450 Total Harmonic Distortion + Noise vs Frequency



1450/50L G11

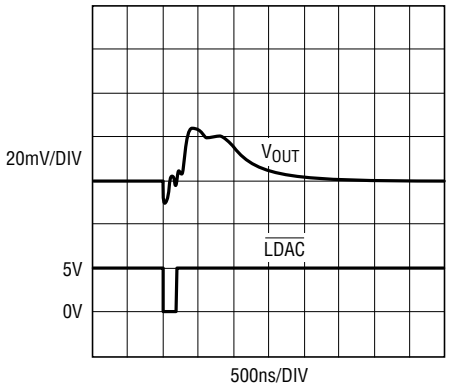
LTC1450 Broadband Output Noise



1450/50L G12

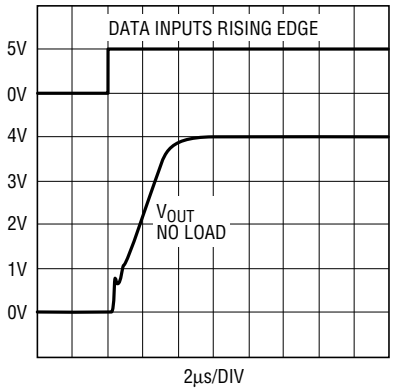
TYPICAL PERFORMANCE CHARACTERISTICS

LTC1450 Midscale Transition
Data = 2048 to 2047



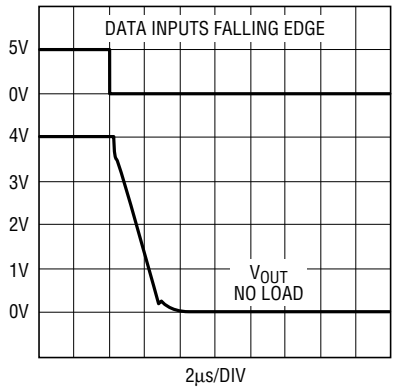
1450/50L G13

LTC1450
Large-Scale Settling (Rising)



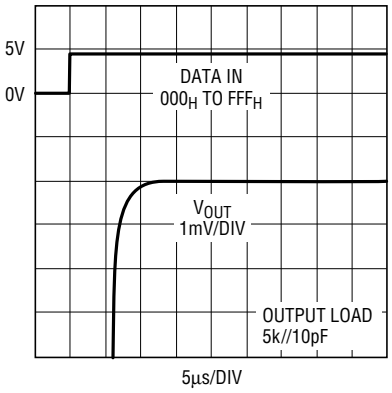
1450/50L G14

LTC1450
Large-Scale Settling (Falling)



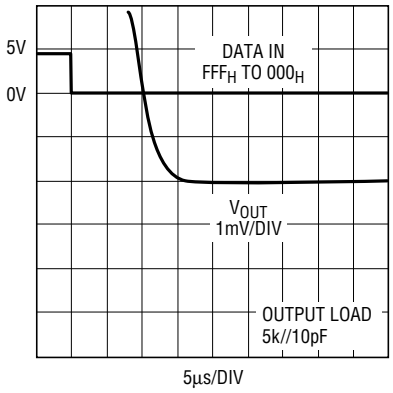
1450/50L G15

Output Voltage Full-Scale Settling



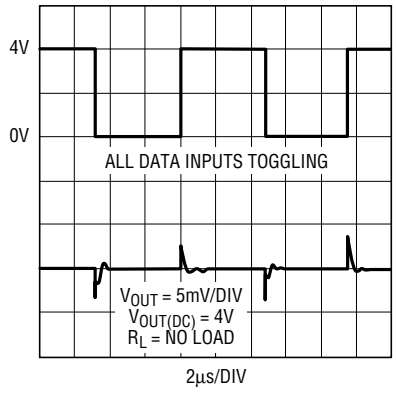
1450/50L G16

Output Voltage Zero-Scale Settling



1450/50L G17

LTC1450 Digital Feedthrough



1450/50L G18

PIN FUNCTIONS

$\overline{WR}$ (Pin 1): Write Input (Active Low). Used with $\overline{CSMSB}$ and/or $\overline{CSLSB}$ to load data into the input latches. While $\overline{WR}$ and $\overline{CSMSB}$ and/or $\overline{CSLSB}$ are held low the enabled input latches are transparent. The rising edge of $\overline{WR}$ will latch data into all input latches.

$\overline{CSLSB}$ (Pin 2): Chip Select Least Significant Byte (Active Low). Used with $\overline{WR}$ to load data into the eight LSB input latches. While $\overline{WR}$ and $\overline{CSLSB}$ are held low the eight LSB input latches are transparent. The rising edge will latch data into the eight LSB input latches. Can be connected to $\overline{CSMSB}$ for simultaneous loading of both sets of input latches on a 12-bit bus.

$\overline{CSMSB}$ (Pin 3): Chip Select Most Significant Byte (Active Low). Used with $\overline{WR}$ to load data into the four MSB input latches. While $\overline{WR}$ and $\overline{CSMSB}$ are held low the four MSB input latches are transparent. The rising edge will latch data into the four MSB input latches. Can be connected to $\overline{CSLSB}$ for simultaneous loading of both sets of input latches on a 12-bit bus.

D0 to D7 (Pins 4 to 11): Input data for the Least Significant Byte. Loaded into LSB input latch when $\overline{WR}$ = 0 and $\overline{CSLSB}$ = 0.

D8, D9, D10, D11 (Pins 12, 13, 14, 15): Input data for the Most Significant Byte. Loaded into MSB input latch when $\overline{WR}$ = 0 and $\overline{CSMSB}$ = 0. Can be connected to D0 to D3 for multiplexed operation on an 8-bit bus.

GND (Pin 16): Ground.

REFLO (Pin 17): Lower input terminal of the DAC's internal resistor string. Typically connected to Analog Ground. An input code of (000_H) will connect the positive input of the output buffer to this end. Can be used to offset the zero scale above ground.

REFHI (Pin 18): Upper input terminal of the DAC's internal resistor string. Typically connected to REFOUT. An input code of (FFF_H) will connect the positive input of the output buffer to 1LSB from this end.

REFOUT (Pin 19): Output of the internal 2.048V/1.22V reference. Typically connected to REFHI to drive internal DAC resistor string.

V_{CC} (Pin 20): Positive Power Supply Input. $4.5V \leq V_{CC} \leq 5.5V$ (LTC1450) and $2.7V \leq V_{CC} \leq 5.5V$ (LTC1450L). Requires a bypass capacitor to ground.

V_{OUT} (Pin 21): Buffered DAC Output.

X1/X2 (Pin 22): Gain Setting Resistor Pin. Connect to GND for G = 2 or to V_{OUT} for G = 1. Should always be tied to a low impedance source, such as ground or V_{OUT}, to ensure stability of the output buffer when driving capacitive loads.

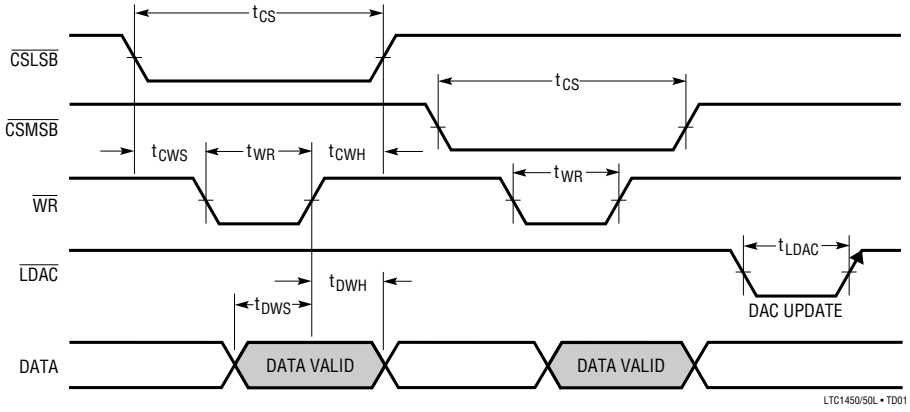
$\overline{CLR}$ (Pin 23): Clear Input (Asynchronous Active Low). A low on this pin asynchronously resets all internal latches to 0s.

$\overline{LDAC}$ (Pin 24): Load DAC (Asynchronous Active Low). Used to asynchronously transfer the contents of the input latches to the DAC latches which updates the output voltage. The rising edge latches the data into the DAC latches. If held low the DAC latches are transparent and data from the input latches will immediately update V_{OUT}.

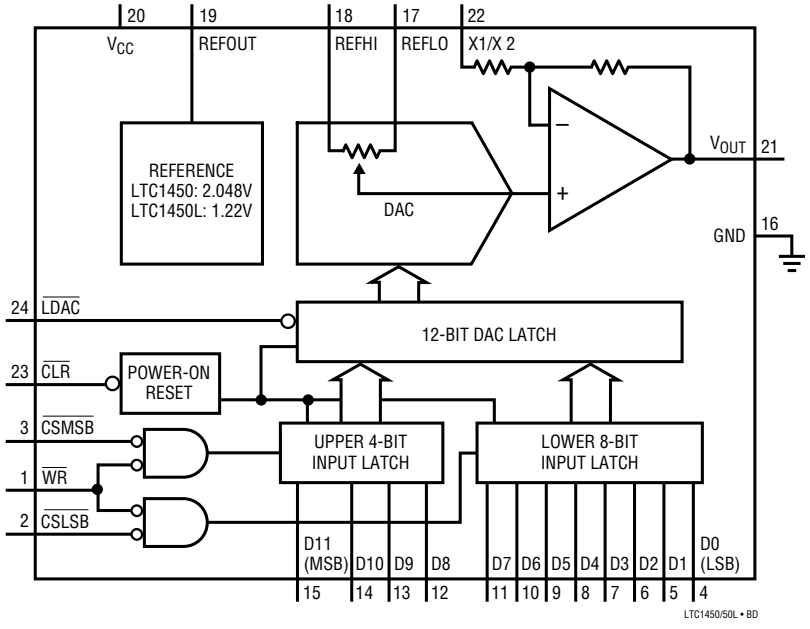
DIGITAL INTERFACE TRUTH TABLE

$\overline{CLR}$	$\overline{CSMSB}$	$\overline{CSLSB}$	$\overline{WR}$	$\overline{LDAC}$	FUNCTION
H	H	L	L	H	Loads the eight LSBs into the input latch
H	H	L	↑	H	Latches the eight LSBs into the input latch
H	H	↑	L	H	Latches the eight LSBs into the input latch
H	L	H	L	H	Loads the four MSBs into the input latch
H	L	H	↑	H	Latches the four MSBs into the input latch
H	↑	H	L	H	Latches the four MSBs into the input latch
H	H	H	H	L	Loads the input latch data into the DAC latch
H	H	H	H	↑	Latches the input latch data into the DAC latch
H	L	L	L	L	Loads input data into DAC latches (latches transparent)
H	L	L	L	↑	Latches input data into DAC latches
L	X	X	X	X	All zeros loaded into input and DAC latches

TIMING DIAGRAM



BLOCK DIAGRAM



DEFINITIONS

Resolution (n): Resolution is defined as the number of digital input bits (n). It defines the number of DAC output states (2^n) that divide the full-scale range. The resolution does not imply linearity.

Full-Scale Voltage (V_{FS}): This is the output of the DAC when all bits are set to 1.

Voltage Offset Error (V_{OS}): The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below zero. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - [(Code)(V_{FS})/(2^n - 1)]$$

Least Significant Bit (LSB): One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS})/(2^n - 1) = (V_{FS} - V_{OS})/4095$$

Nominal LSBs:

LTC1450 LSB = 4.095V/4095 = 1mV
LTC1450L LSB = 2.5V/4095 = 0.610mV

Integral Nonlinearity (INL): End-point INL is the maximum deviation from a straight line passing through the end points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below zero, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows:

$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/4095)]/LSB$
V_{OUT} = The output voltage of the DAC measured at the given input code

Differential Nonlinearity (DNL): DNL is the difference between the measured change and the ideal one LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$DNL = (\Delta V_{OUT} - LSB)/LSB$
ΔV_{OUT} = The measured voltage difference between two adjacent codes

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in (nV)(s).

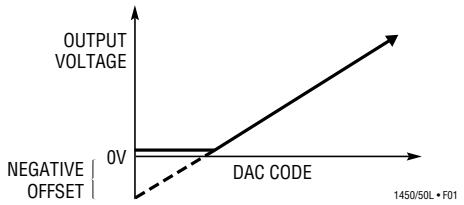


Figure 1. Effect of Negative Offset

OPERATION

Parallel Interface

The data on the input of the DAC is loaded into the DAC's input latches when Chip Select ($\overline{CSLSB}$ and/or $\overline{CSMSB}$) and $\overline{WR}$ are at a logic low. The data that is loaded into the input latches will depend on which of the Chip Selects are at a logic low (see Digital Interface Truth Table). If $\overline{WR}$ and $\overline{CSLSB}$ are both low and $\overline{CSMSB}$ is high, then only data on the eight LSBs (D0 to D7) is loaded into the input latches. Similarly if $\overline{WR}$ and $\overline{CSMSB}$ are both low and $\overline{CSLSB}$ is high then only data on the four MSBs (D8 to D11) is loaded into the input latches. Data is loaded into both the Least Significant Data Bits (D0 to D7) and the Most Significant Bits (D8 to D11) at the same time if $\overline{WR}$, $\overline{CSLSB}$ and $\overline{CSMSB}$ are low.

The input data is latched into the input latches on the rising edge of either the $\overline{WR}$ or one of the Chip Selects. The $\overline{WR}$ transition high will latch the data in both input latches. A rising edge on $\overline{CSMSB}$ will latch data bits D8 to D11. A rising edge on $\overline{CSLSB}$ will latch data bits D0 to D7.

Once data is loaded into the input latches, it can be loaded into the DAC latch. This will update the analog voltage output of the DAC. The DAC latch is loaded by a logic low on $\overline{LDAC}$. The data that is loaded into the DAC latch will be latched on the rising edge of $\overline{LDAC}$.

When $\overline{WR}$, $\overline{CSLSB}$, $\overline{CSMSB}$ and $\overline{LDAC}$ are all low the latches are transparent and data on pins D0 to D11 loads directly into the DAC latch.

Power-On Reset

The LTC1450/LTC1450L have an internal power-on reset that resets all internal latches to 0's on power-up (equivalent to the $\overline{CLR}$ pin function).

Reference

The LTC1450 includes an internal 2.048V reference, giving the LTC1450 a full-scale range of 4.095V in the gain of 2 configuration. The LTC1450L has an internal 1.22V reference with a full-scale range of 2.5V and a gain of 2.05 in the gain of 2 configuration. The onboard reference in the LTC1450 and LTC1450L is not internally connected to the DAC's reference resistor string but is provided on an adjacent pin for flexibility. Because the internal reference is not internally connected to the DAC resistor string, an external reference can be used or the resistor string can be driven with an external source in multiplying configuration. The external reference or source must be capable of driving the 8k minimum DAC ladder resistance.

The reference output noise can be reduced with a bypass capacitor to ground. (Note: The reference does not require a bypass capacitor to ground for proper operation.) When bypassing the reference a small value resistor in series with the capacitor is recommended to help reduce peaking on the output. A 10Ω resistor in series with a 4.7μF capacitor is optimum for reducing reference generated noise.

DAC Ladder Resistor String

The high and low end of the DAC ladder resistor string (REFHI and REFLO respectively) are not connected internally on this part. Typically REFHI will be connected to REFOUT and REFLO will be connected to GND. This will give the LTC1450 a full-scale range of 4.095V. The full-scale range for the LTC1450L will be 2.5V

Either of these pins can be driven up to V_{CC} – 1.5V when using the buffer in the gain of 1 configuration. The resistor string pins can be driven to $V_{CC}/2$ when the buffer is in the gain of 2 configuration (2.05 for the LTC1450L). The resistance between these two pins is typically 18k (8k min).

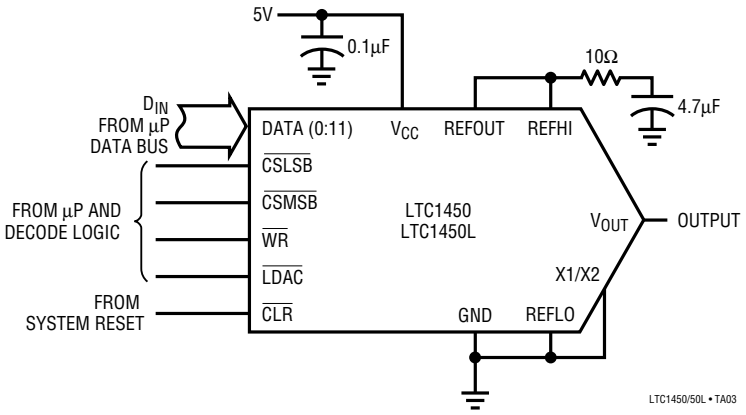
Voltage Output

The output buffer for the LTC1450/LTC1450L can be configured for two different gain settings. By tying the X1/X2 pin to GND the gain is set to 2 (2.05 for the LTC1450L). By tying the X1/X2 pin to V_{OUT} the gain is set to one.

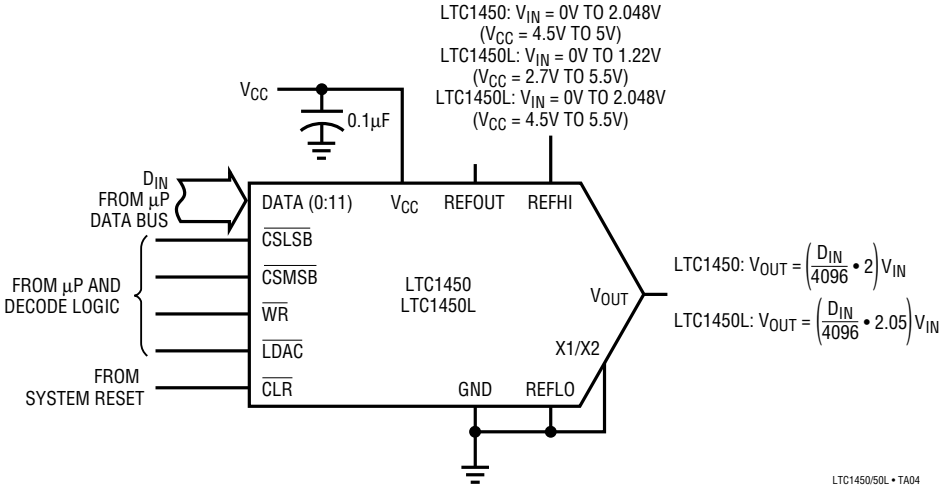
The LTC1450 family's rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or GND. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40Ω when driving a load to the rails.

TYPICAL APPLICATIONS

Filter V_{REF} to Lower Output Noise (0.18mV_{RMS} at V_{OUT})

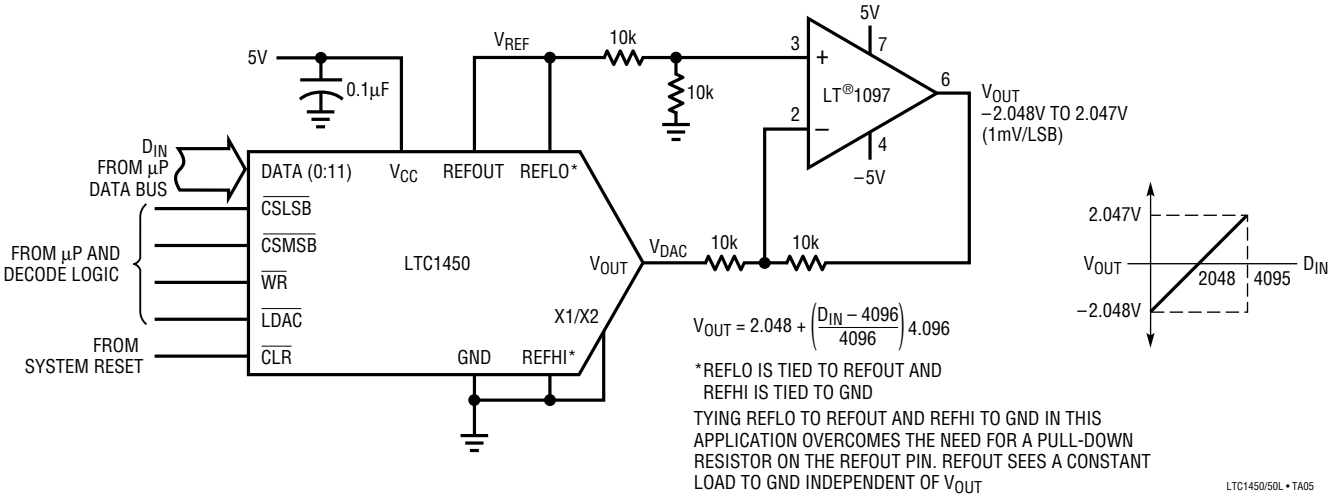


Digitally Programmable Noninverting Amplifier



TYPICAL APPLICATIONS

Bipolar Output 12-Bit DAC



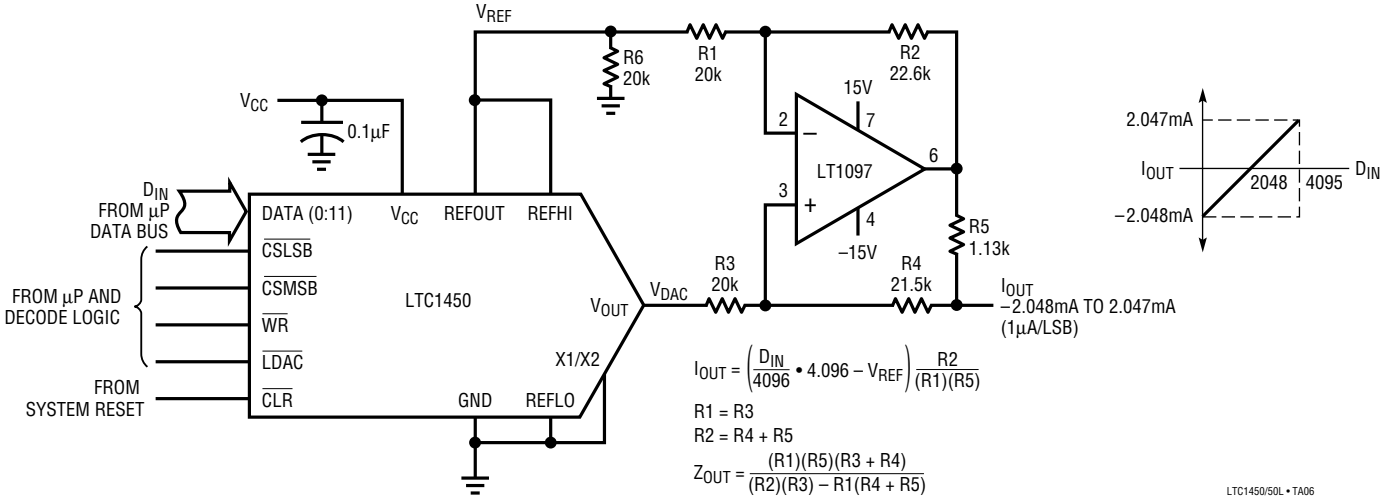
$$V_{OUT} = 2.048 + \left(\frac{D_{IN} - 4096}{4096}\right) 4.096$$

*REFLO IS TIED TO REFOUT AND REFHI IS TIED TO GND

TYING REFLO TO REFOUT AND REFHI TO GND IN THIS APPLICATION OVERCOMES THE NEED FOR A PULL-DOWN RESISTOR ON THE REFOUT PIN. REFOUT SEES A CONSTANT LOAD TO GND INDEPENDENT OF V_{OUT}

LTC1450/50L • TA05

Digitally Programmable Bilateral Current Source/Sink



$$I_{OUT} = \left(\frac{D_{IN}}{4096} \bullet 4.096 - V_{REF}\right) \frac{R2}{(R1)(R5)}$$

R1 = R3

R2 = R4 + R5

$$Z_{OUT} = \frac{(R1)(R5)(R3 + R4)}{(R2)(R3) - R1(R4 + R5)}$$

LTC1450/50L • TA06

TYPICAL APPLICATIONS

4-Quadrant Multiplying DAC Application

This application shows the LTC1450L configured as a single supply 4-quadrant multiplying DAC. It uses a 5V supply and only one external component, a 5k resistor tied from REFOUT to ground. (The LTC1450 can be used in a similar fashion.) The multiplying DAC allows the user to digitally change the amplitude and polarity of an AC input signal whose voltage is centered around an offset signal ground provided by the 1.22V reference voltage. The transfer function is shown in the following equations.

$$V_{OUT} = (V_{IN} - V_{REF}) \left[Gain \left(\frac{D_{IN}}{4096} - 1 \right) + 1 \right] + V_{REF}$$

For the LTC1450L Gain = 2.05 and V_{REF} = 1.22V

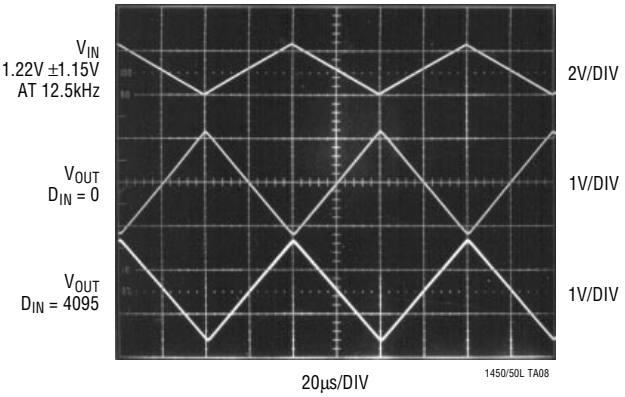
$$V_{OUT} = (V_{IN} - 1.22V) \left[2.05 \left(\frac{D_{IN}}{4096} \right) - 1.05 \right] + 1.22V$$

Table 1 shows the expressions for V_{OUT} as a function of V_{IN}, V_{REF} and D_{IN}. The scope photo shows a 12.5kHz, $2.3V_{P-P}$ triangle wave input signal and the corresponding output waveforms for zero-scale and full-scale DAC codes.

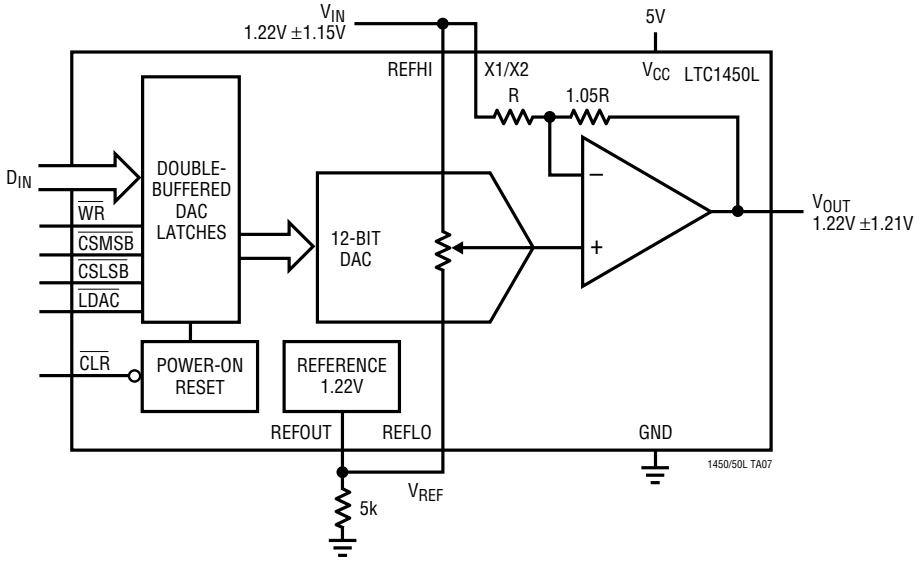
Table 1. Binary Code Table for 4-Quadrant, Multiplying DAC Application

BINARY DIGITAL INPUT CODE IN DAC REGISTER			ANALOG OUTPUT (V_{OUT})
MSB		LSB	
1111	1111	1111	$(4094/4096)(V_{IN} - V_{REF}) + V_{REF}$
1100	0001	1001	$0.5(V_{IN} - V_{REF}) + V_{REF}$
1000	0011	0010	V_{REF}
0100	0100	1011	$-0.5(V_{IN} - V_{REF}) + V_{REF}$
0000	0110	0100	$-1.0(V_{IN} - V_{REF}) + V_{REF}$
0000	0000	0000	$-1.05(V_{IN} - V_{REF}) + V_{REF}$

Clean 4-Quadrant Multiplying Is Shown in the Output Waveforms for Zero-Scale and Full-Scale DAC Settings



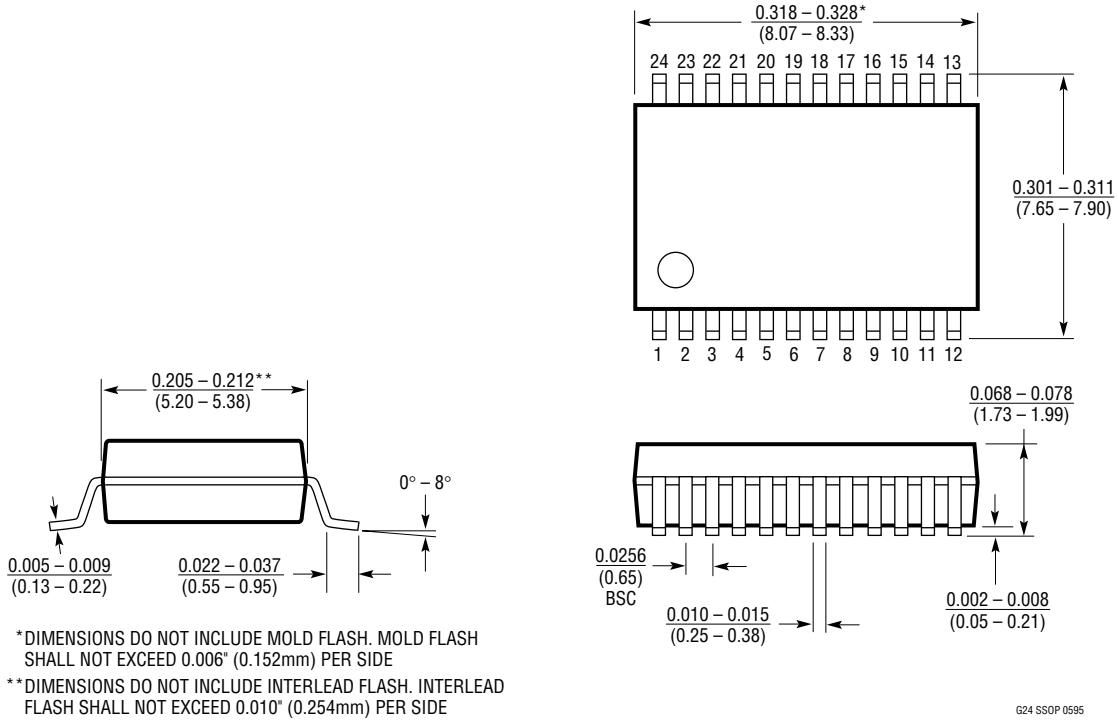
Internal Reference, REFLO/REFHI Pins, Gain Adjust and Wide Supply Voltage Range Allow 4-Quadrant Mulitplying on a 5V Single Supply



PACKAGE DESCRIPTION

Dimensions in Inches (millimeters) unless otherwise noted.

G Package
24-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



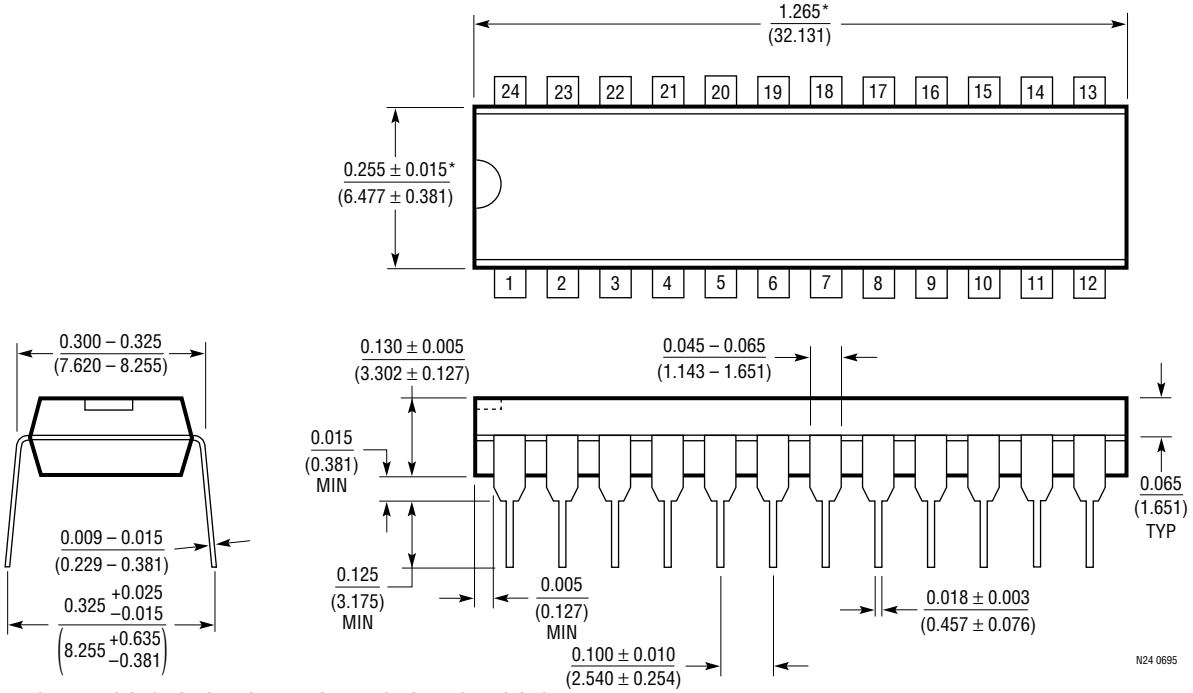
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

N Package
24-Lead PDIP (Narrow 0.300)
(LTC DWG # 05-08-1510)



*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.010 INCH (0.254mm)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1257	Complete Serial I/O V_{OUT} 12-Bit DAC	5V to 15V Single Supply in 8-Pin SO and PDIP
LTC1451/LTC1452/LTC1453	Complete Serial I/O V_{OUT} 12-Bit DACs	3V/5V Single Supply, Rail-to-Rail in 8-Pin SO and PDIP
LTC1446/LTC1446L	Dual 12-Bit V_{OUT} DACs in SO-8 Package	LTC1446: V_{CC} = 4.5V TO 5.5V, V_{OUT} = 0V TO 4.095V LTC1446L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1454/LTC1454L	Dual 12-Bit V_{OUT} DACs in a 16-Pin SO Package with Added Functionality	LTC1454: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V TO 4.095V LTC1454L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC1458/LTC1458L	Quad 12-Bit V_{OUT} DACs in 28-Lead SW and SSOP Packages	LTC1458: V_{CC} = 4.5V to 5.5V, V_{OUT} = 0V to 4.095V LTC1458L: V_{CC} = 2.7V to 5.5V, V_{OUT} = 0V to 2.5V
LTC7541A	Parallel I/O Multiplying 12-Bit DAC	12-Bit Wide Input
LTC7543/LTC8143	Serial Multiplying 12-Bit DACs	Daisy-Chainable, Flexible Analog and Digital Interface
LTC7545A	Parallel Latched Input Multiplying 12-Bit DAC	12-Bit Wide Latched Input
LTC8043	Serial Multiplying 12-Bit DAC	8-Pin SO and PDIP

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